

PS-FPG: Pattern Selection based co-design of Floorplan and Power/Ground Network with Wiring Resource Optimization

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Abstract - As technology advances, the voltage (IR) drop in the Power/Ground (P/G) network becomes a serious problem in modern IC design. The P/G network co-design with floorplan can improve the power design quality. Different with traditional approaches which analyze P/G network during the floorplanning iterations, in this paper, an efficient pattern selection method is used to provide gradient information for fast signal-integrity estimation. We also propose a novel P/G aware incremental algorithm which can intelligently fix the violations during the floorplanning process. The P/G pin assignment and wire sizing method are adopted during the floorplanning process so that the power routing resource can be minimized with the constraints of IR drop and electron migration (EM) considered. Experimental results based on the MCNC benchmarks show that our design not only significantly speeds up the optimization process, but also optimizes the power routing resource while the quality of the floorplanning is maintained.

I. Introduction

As technology advances, the threshold voltage scales nonlinearly, raising the ratio of the threshold voltage to the supply voltage and making IR drop in the P/G network a serious challenge. The reduced supply voltages and on-chip supply variation due to the significant IR drop may weaken the driving capability of logical gates, reduce circuit performance and lower noise margin [7]. As the design complexity increases dramatically, it is necessary to handle the IR drop problem earlier in the design cycle for better design convergence. To optimize the P/G network distribution, we normally consider the following two factors: 1) The packing of modules influences the IR drop distribution of the whole chip greatly; 2) Increasing wire width of P/G network can help to reduce the IR drop, but the wiring resources are limited in modern designs. Hence, it is necessary to optimize the floorplanning and P/G network simultaneously with the wiring resources considered.

A. Co-optimization of Packing and P/G network

The packing of modules influences the IR drop distribution greatly. Fig.1 shows the packing of a chip and its P/G network. We refer to a pad feeding supply voltage into the chip as a *power pad*, the power line enclosing the floorplan as a *core ring*, a power line branching from a core ring into modules inside as a *power trunk*, an intersection of a vertical and a horizontal power lines as a *P/G node*, and a pin in a module that absorbs current (connects to a core ring or a power trunk) as a *P/G pin*. Fig. 1(a) shows an instance of voltage drop in the power supply in which the voltage drops by almost 26% at the rightmost P/G pin. But the packing in Fig. 1(b) has smaller worst-case voltage drop. Therefore, it is desired to consider the P/G network design during early physical design (e.g., floorplanning) for reliable circuit operation.

Several recent works [1-5] considered the P/G network analysis in the floorplanning stage using different topologies for

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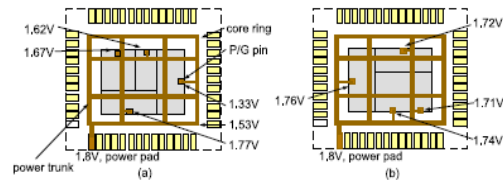


Fig. 1: (a) the packing of a chip and its P/G network structure. The worst-case voltage at the P/G pins is about 26% of the supply voltage; (b) a floorplan with smaller worst-case IR drops. The worst-case IR drop is about only 5%.

P/G network, such as tree structure, uniform mesh and non-uniform mesh. Wu and Chang [2] viewed P/G networks as binary trees during the floorplanning process. Although the tree based P/G network can minimize the wiring resources, it is unreliable because the power pad only has one way to connect to the current sources. Once EM happened in one power wire, the whole P/G network will fail. In [5], Wang proposed a method to generate a non-uniform power supply mesh network. It saves the routing resources of P/G network, but the disadvantage of this approach is that the non-uniform network would increase the complexity in the routing process. The uniform mesh structure is widely used for P/G network since it is reliable and easy for signal router. In this paper, we focus our research on the uniform mesh structure. But for the uniform mesh structure, the IR drop estimation in each floorplan iteration leads to obvious time overhead to solve the linear system. [14] proposed a pattern selection based approach to speed up the P/G analysis, but still the floorplanning process based on stochastic optimization may suffer from poor convergence. To speed up the searching process of P/G network and floorplan co-design, Liu [1] constrained some power-hungry modules to be along the boundaries so that the IR drop constraints can be met. Although it can improve the speed of the whole search process due to the reduction of the solution space, it may over-constrain the modules since the power-hungry modules are not necessarily to be located along the boundary to meet the IR-drop constraint. Consequently, the approach in [1] may lose the ability to obtain the optimized feasible results. So the co-optimization of floorplanning and P/G network needs not only an efficient P/G network analysis method, but also an intelligent floorplanning scheme so that the optimization process can be converged efficiently.

B. Wire sizing for P/G network

Besides the P/G aware floorplanning, wire sizing can also be used to reduce the severe IR drop. An important problem of P/G network synthesis is to use the minimum amount of wiring area for a P/G network under the power-integrity constraints such as IR drops and EM. Recently, many literatures [10-13] used the wire sizing method to optimize the wiring resources. They all assume that the topologies of P/G networks are fixed so that only the widths of the wire segments need to be

determined in the post-floorplan stage. But the packings influence the IR drop distribution as well as the wire sizing results. The packing regions with serious current load need wider wire segments to reduce the IR drop. Similarly, the packing region with small current load can use thinner wire segments to minimize the wire resources. So it is effective and reasonable to embed the wire sizing method into the floorplan process. In work [1], they modified the P/G mesh network combined with the feasible floorplan by changing the size of each mesh grid to meet the IR drop and EM constraints. But it would cause over-density of the power grids in some regions where the current loads are serious. Furthermore, they did not consider the wiring resources co-optimization with floorplanning.

C. Our contribution

In co-design of floorplanning and P/G network planning, we need not only an efficient, effective, and flexible floorplanning algorithm, but also a very efficient, yet sufficiently accurate P/G network analysis method. The structure of the P/G network is somewhat regular which can be scaled to match different packings. Therefore, instead of analyzing the P/G network by solving equations in each iteration, in this paper, we set up a pattern selection scheme in which the useful gradient information of many kinds of P/G network patterns are installed for fast signal-integrity estimation. Using pattern selection method can significantly speed up the optimization process by avoiding repeatedly calculating complex matrix inverse. We also propose a guided incremental floorplanning approach, in which the IR drop violations can be amended intelligently during the floorplanning process based on B*-tree representation. At the same time, to minimize the area of P/G network with considering IR voltage drop and EM, the P/G pin assignment and the wire sizing method are also embedded in the floorplanning optimization process. Compared with other traditional approaches, our method has following advantages:

- Our algorithm uses the pattern selection method which can speed up the optimization process by avoiding repeatedly calculating complex matrix inverse.
- To further speed up the process, unlike [1] which may lose the ability to find the optimal packing due to the reduction of solution space, we use the P/G network aware incremental moves to amend the violated constraints. Our approach can amend the violations incrementally in a complete packing solution space.
- Beside the co-optimization of P/G network with floorplanning, the wire sizing method and P/G pins assignment are also adopted to minimize the power wire resource with considering the IR drop and EM constraints.

II. Problem Formulation

The problem of floorplan and P/G network co-design is formulated as follows: Given a floorplan of m modules, the number of power pads for the whole chip and the power consumption for each module, the objective is to obtain a feasible floorplan and simultaneously generate a corresponding P/G network with minimal wiring resource while the power constraints are satisfied. We introduce the notations for describing a P/G network: Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, 2, \dots, n\}$ and b branches $B = \{1, 2, \dots, b\}$. Each branch b_i in B connects two nodes: n_{i1} and n_{i2} with current flowing from n_{i1} to n_{i2} . Let l_i and w_i be the length and

width of branch b_i , respectively. Let ρ be the sheet resistivity (unit Ω per square), and $V_i(I_i)$ be the voltage (current) at node n_i . Then the resistance r_i of branch b_i is $r_i = (V_{i1} - V_{i2})/I_i = \rho * l_i / w_i$. At the early stage of power analysis, we need an efficient analysis for the P/G network. For this reason, a sophisticated model for the P/G network is often too time-consuming and thus infeasible for the co-design. In this paper, we use the resistive model for P/G networks and the static current source model. We consider the power integrity constraints as follows:

• The IR-drop constraints:

For every P/G pin p_i , its corresponding voltage V_{p_i} must satisfy the following constraints:

$$\begin{aligned} V_{p_i} &\geq V_{min,k}; \text{ for each power pin } i \text{ of module } k, \\ V_{p_i} &\leq V_{max,k}; \text{ for each ground pin } i \text{ of module } k, \end{aligned}$$

Where $V_{min,k}(V_{max,k})$ is the minimum (maximum) voltage required at injection point of a P/G network for module k .

• The minimum width constraints:

The width of a P/G line b_i connecting nodes n_{i1} and n_{i2} must be greater than the minimum width in the given technology. The constraint is given by:

$$w_i = \frac{\rho * l_i * I_i}{V_{i1} - V_{i2}} \geq w_{i,min} \quad (1)$$

Where $w_{i,min}$ is the given constraint.

• The electromigration constraints:

$$|V_{i1} - V_{i2}| \leq \rho * l_i * \sigma \quad (2)$$

Where σ is a constant for a particular routing layer with a fixed thickness.

In our formulation, the overall cost function contains four terms. The term $A(s)$ is used to describe the floorplan area, the term $W(s)$ is used to describe the total wire length, the term $A_p(s)$ represents the metal resources used by P/G network in the constraint of IR drop and EM and the term $\phi(s)$ represents the penalty function of the IR drop and EM constraints (for more detailed explanations of this function, please see [1]).

$$\begin{aligned} \min_s \quad & \lambda_1 A(s) + \lambda_2 W(s) + \lambda_3 A_p(s) + \lambda_4 \phi(s) \\ \text{where } \sum_{k=1}^4 \lambda_k &= 1, 0 < \lambda_k < 1 (1 \leq k \leq 4) \end{aligned} \quad (3)$$

And for a given floorplan s , the metal resource $A_p(s)$ is defined as follows:

$$\begin{aligned} \min \quad & A_p = \sum_{i=1}^b l_i \times w_i \\ \text{s.t. } \quad & V_{worst} \leq V_t, \quad D_{max} \leq D_t \end{aligned} \quad (4)$$

where V_{worst} is the worst IR drop, V_t is the IR drop tolerance, D_{max} is the max branch current density, and D_t is the branch current density tolerance representing EM constraints and l_i and w_i be the length and width of branch i , respectively.

III. P/G Network Analysis Using Mesh Pattern

To obtain power integrity violations, we firstly construct a P/G mesh for a given floorplan and then evaluate the P/G mesh for IR drop and EM effects. To obtain a reasonable mesh structure, we adopt the P/G network analysis using pattern selection method. Before the packing optimization process, we create a regular power network pattern table to provide gradient information for fast estimation.

A. P/G Network Structure

In order to evaluate the performance of the actual P/G network of a given floorplan at the floorplanning stage, we

generate a conceptual P/G network for the floorplan. A uniform mesh can be generated easily by evenly distributing the power lines as shown in Fig. 2(a). To reduce the complexity, we make a reasonable approximation by attaching all current sources to the intersection nodes of the vertical and horizontal power lines. That is, every P/G pin is connected to its nearest node with a power strap. For convenience, we divide the floorplan into n regions, where n is the number of the nodes as shown in Fig. 2(a). The border line of two regions is the center line between the two nodes such that the node is the nearest one for any point in the region.

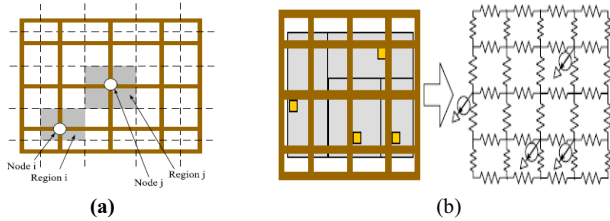


Fig. 2 (a) A floorplan with a P/G mesh divided into regions, (b) A power mesh and its equal circuit model

B. P/G Network Analysis

When we obtain a P/G network, we analyze the P/G mesh with the floorplan. Traditional analysis method is very computationally expensive [1]. We apply the resistive P/G network model and use the maximum current drawn by the modules for static P/G network analysis. As the P/G mesh example shown in Fig. 2(b), the chip is composed of four modules. The P/G wires are modeled as resistors. A P/G pin in a hard module is modeled as a current source. The static analysis of a P/G network is formulated:

$$\mathbf{G} \mathbf{x} = \mathbf{i} \quad (5)$$

Where \mathbf{G} is the conductance matrix for the resistors, \mathbf{x} is the vector of node voltages, and \mathbf{i} is the vector of current loads. The dimensions of \mathbf{i} and \mathbf{x} are equal to the number of nodes in the P/G network. So we can use the following equation to solve the voltage of each node. Once the voltage of each node is obtained, we can estimate the voltage at each P/G pin based on the voltage of the closest node.

$$\mathbf{x} = \mathbf{G}^{-1} \mathbf{i} \quad (6)$$

C. P/G Mesh Patterns

From equation (6), we can see that computing the converse of the conductance matrix for the resistor of the P/G network is the major work. Given a certain P/G network, the conductance matrix is unchanged. We know that if \mathbf{G}^{-1} is computed, we can easily obtain the voltage for each node in P/G mesh network, the IR drop can also be known easily. So if we can pre-compute \mathbf{G}^{-1} before floorplanning optimization, it will speed up the iterative process, without repeatedly calculating complex matrix inverse. The difficult issue is how to decide the size of the P/G mesh network before the floorplan is generated. Normally, the aspect ratio of a feasible floorplan is varied from 1:3 to 3:1 in the whole search process. Therefore, we can create some patterns. As shown in Fig. 4, we create sixteen kinds of P/G mesh network whose sizes are from 3*3 to 18*18. Furthermore, we divide six kinds of choices such as 1:3, 1:2, 1:1, 1.5:1, 2:1, 2.5:1 and 3:1 as the aspect ratio of the P/G mesh network according to the different floorplan generated in the search process. We establish a pattern table to record the useful information such as the \mathbf{G}^{-1} and so on. Therefore, there are 112

kinds of patterns. Each P/G mesh network pattern can be scaled to match a feasible floorplan. Similarly, once we obtain a feasible floorplan, we can choose an appropriate pattern from the P/G mesh network pattern table according to the aspect ratio. It can greatly reduce the run time of analysis for the P/G network, thus the co-design process using pattern selection method can be very efficient.

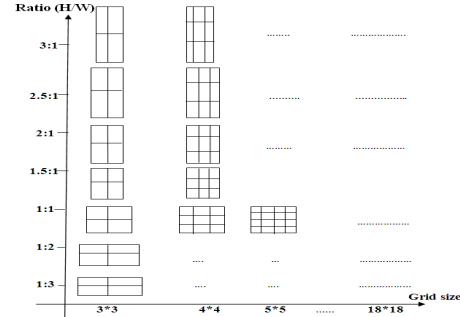


Fig.4 The P/G mesh pattern table

IV. P/G Network Aware Incremental Moves

Among the power integrity constraints, IR-drop is the most complicated. Based on the circuit theory, the IR-drop of a P/G pin is proportional to the effective resistance between the P/G pin and the power pad. Therefore, the closer the P/G pin is placed to the power pad, the smaller IR drop we can get. In our implementation, we give each circuit two power pads located on the left-bottom corner and top-right corner respectively as shown in Fig. 5(a). So we can move the violating modules close to the two corners to fix the violations.

Our P/G aware incremental algorithm uses the Simulate Annealing-based algorithm with the B*-tree floorplan representation [6]. Given an admissible placement, we can construct a unique B*-tree. Fig. 5(a) shows an admissible placement and its corresponding B*-tree illustrated in Fig. 5(b).

A B*-tree is an ordered binary tree whose root corresponds to the module on the bottom-left corner. Similar to the depth-first search (DFS) procedure, we construct a B*-tree T for an admissible placement in a recursive fashion: Starting from the root, we first recursively construct the left subtree and then the right subtree. Let R_i denote the set of modules located on the right-hand side and adjacent to m_i . The left child of the node n_i corresponds to the lowest module in R_i that is unvisited. The right child of n_i represents the lowest module located above and with its x -coordinate equal to that of m_i .

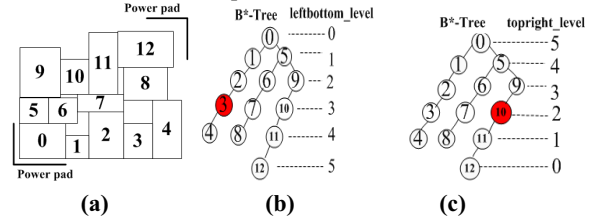


Fig. 5: (a) An admissible placement; (b) The corresponding B*-tree of (a) and the *leftbottom_level* representation; (c) The corresponding B*-tree of (a) and the *topright_level* representation

From the construction of B*-tree, we can see that the lower level where a node exists, the closer the module to the root modules in topological relations. Such as in Fig. 5, modules 1 and 5, which are at level 1 in the tree, are closer to the lower-left corner than modules 2, 6 and 9, which are at level 2.

At the same time, we have another power pad which is at the upper-right corner. The module at the upper-right corner should correspond to the node with the deepest level in B*-tree, such as module 12 in Fig.5. To represent the topological distance to the upper-right corner, we also count the level in B*-tree reversely. Therefore, we accordingly devise two kinds of level representations which are called *leftbottom_level* and *topright_level* respectively. As shown in Fig. 5(b), we can traverse a B*-tree in level order and obtain the *leftbottom_level* for each module. As shown in Fig.5(c), we traverse a B*-tree and visit the nodes from the leaf level to the root level, and then obtain the *topright_level* for each module. According to the two kinds of level representations, we can see that the modules corresponding to the nodes on lower levels are placed close to the corresponding power pad.

As we all know, the final placement not only depends on B*-tree structure, but also depends on the dimension of the modules. Therefore, we use the coordinates of the violating modules to calculate distances to the two power pads respectively. To fix the violations, we choose to move the violating modules towards the closer power pad. The corresponding level information can guide the movement. For example, when the left-bottom power pad is closer to the violating module, we would move a violating node to lower levels using the *leftbottom_level* representation. Besides the normally used moves in B*-tree based optimization, we introduce two incremental moves given by follows:

Incre_Op1: Select a violating node to swap with another node which is on lower levels;

Incre_Op2: Select a node on the lower levels and insert the violating node as the child of it, and then maintain the violating node on the lower level after this operation.

For example, if n_3 violates the IR-drop constraint as shown in Fig. 5(a), we can see that the left-bottom power pad is close to the module 3. So we do the incremental changes like **Incre_Op1** or **Incre_Op2** using the *leftbottom_level* representation as shown in Fig. 5(b). If we do the **Incre_Op1**, we choose a node on lower levels to swap, such as n_0 , n_1 , n_5 and so on. Doing the **Incre_Op2**, we firstly delete n_3 and then choose n_0 , n_1 or n_5 as the father of it. After this operation, n_3 should be on level 1 or level 2.

If n_{10} violates the IR drop constraint, we can figure out the distance between module 10 and two power pads. Since module 10 is close to the top-right power pad. So we can do the incremental changes using the *topright_level* representation as shown in Fig. 5(c). Doing the **Incre_Op1**, we select n_4 , n_8 , n_{11} or n_{12} to swap with n_{10} . If we do the **Incre_Op2**, we can first delete n_{10} and choose n_4 , n_8 , n_{11} or n_{12} as the father of it. After this operation, n_{10} is on level 0 or level 1.

These two operations give some guidelines to fix the infeasible solutions when the violation is detected. It is easier to generate legal solutions than random moves completely. So the efficiency of the search can be improved maintaining the complete solution space.

V. The Co-Design Algorithm Flow

The flow of our co-design algorithm is summarized in Fig.6. Firstly, we construct the P/G network mesh patterns mentioned in section III to establish a P/G mesh network pattern table. Given an initial floorplan, we select an appropriate mesh

network pattern using the pattern selection method. We adopt an effective P/G pin assignment algorithm after the P/G mesh network selected. Then we estimate the IR drop of each module. If the IR drop constraint is not satisfied, we can broaden the power wire width in a certain range. At the same time, when the worst IR drop is smaller than the target IR drop, we can reduce the width of the power wire to minimize the P/G wiring resources. If the constraints are still not satisfied after using wire sizing method, we can change to another mesh pattern. In the co-design process, we also add the guided P/G network aware incremental move method into the simulated annealing algorithm with the B*-tree representation. The whole process repeats until the termination conditions are met.

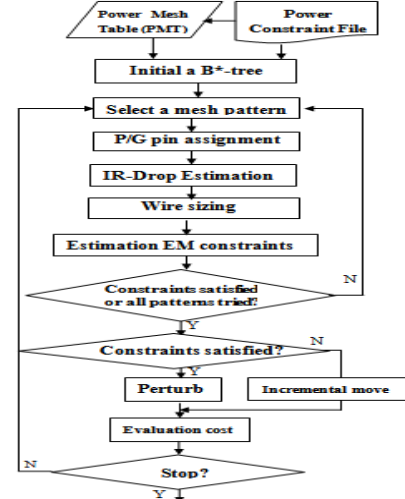


Fig. 6 The flow of our co-design algorithm

A. Pattern Selection

Given a feasible floorplan, we can search the power mesh table to find a proper mesh pattern whose aspect ratio is close to the given floorplan. But some time the width and height are not completely consistent. So we need to scale the selected mesh pattern according to a certain proportion. As shown in Fig. 7(b), for example, the dashed line stands for the network in P/G mesh network pattern table and the solid line denotes the network magnifying according to the floorplan. Normally, the P/G network is always larger than the floorplan slightly.

When we scale the P/G network k times, the conductive matrix G is also proportional. So the converse of the conductive matrix G^{-1} is proportional, as well. Therefore, once a floorplan is generated, we can select an appropriate P/G network and scale it. When the width and height of the P/G network are magnified k times, each resistance is also magnified k times. So the matrix G is as $1/k$ times as before. According to the matrix knowledge, we can see G^{-1} is magnified k times. Adjusting the size of the network does not increase the time cost of the P/G network analysis, meanwhile, we can find reasonable P/G mesh pattern for all the feasible packings.

In our mesh pattern selection process, we first determine the aspect ratio of the mesh according to the given floorplan. To obtain the minimal wiring resource, we first choose the 3*3 mesh pattern with the aspect ratio which we chose before. And then we can analyze the IR drop and EM constraints using the information of the selected pattern. If there are still violations in P/G network after the wire sizing, we can change to another mesh pattern with the same aspect ratio in sequence.

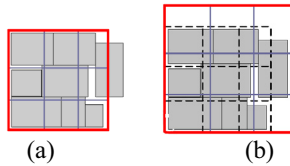


Fig. 7 Adjust the size of P/G mesh network

B. P/G Pin Assignment

The positions of P/G pins of each module may not be fixed in the early design stage. In the floorplan and P/G network co-design, the locations of P/G pins of each module influence the IR drop of the whole chip. In this paper, we assume each module has one P/G pin. We proposed an effective algorithm to do the P/G pin assignment uniformly and reasonably close to the nearby power pad.

In Fig.8 (a), it shows two possible locations of P/G pin of the module 1 connecting with different power nodes. When the P/G pin of module *M1* is placed at the left-bottom corner like *p1*, it connects with power node with less IR drop. If we place the P/G pin of *M1* at the up-right corner like *p2*, it connects with the power node with larger IR drop. In some cases when several P/G pins which connect to the same power node as shown in Fig.8 (b), it would increase the current load of this power node and increase the IR drop. So we want to assign the P/G pins uniformly to the nearby power node.

According to the region information of a selected mesh pattern and the given floorplan, we calculate distances between each module and the two power pads respectively. When one module is near to the bottom-left corner, we assign its P/G pin near to the bottom-left corner and vice versa. Since the IR drops are severe in the middle of the chip, we firstly handle the P/G pins of the modules which are far away from the corresponding power pad. And go towards lower-left corner till the lower left corner is met. Then back to the center and go towards upper-right corner till all the modules are met. Like Fig.8 shows, we firstly focus on module *M2* and determine the position of its P/G pin. We select a power node which it can be connected to *M2* and nearest to the left-bottom power pad. And then we handle *M1*, *M3*, and *M4* in sequence. When we choose a power node which had been occupied by the other P/G pin, we can select the available power node nearby so that the distribution of P/G pins can be evened and the situation as shown in Fig. 8(b) can be avoided.

C. Wire Sizing for the P/G mesh network

After the P/G pins of modules are fixed by the pin assignment algorithm, we can compute the voltage of all power nodes and find out the violations of IR-drop constraints. We apply the wire sizing method to amend the IR drop violations in the co-design process. When all nodes meet their corresponding constraints, we reduce the power wire width to minimize the P/G resource area. As the formulation below:

$$\text{Width_fact} = \frac{\text{Worst_IR}}{\text{Target_IR}} \quad (7)$$

Width_fact determines the width of the P/G network wires after the wire sizing. Increasing the width of the P/G network wires can decrease the voltage. So the IR drop will reduce. On the contrary, the smaller the width of power wire, the larger the IR drop. *Width_fact* is in a certain range that *Width_fact* should be larger than the minimal width and smaller than the maximal width which is given by the constraint file. *Worst_IR* stands for

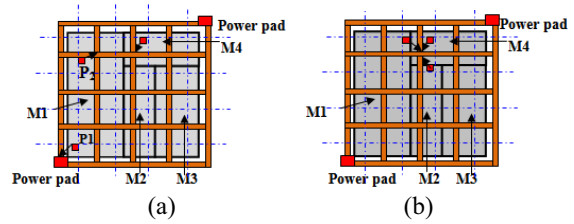


Fig 8: (a) two possible locations of the P/G pin of one module; (b) several pins connect to one power node

the worst IR drop at the present. *Target_IR* denotes the maximal allowable IR drop. When *Worst_IR* = *Target_IR*, no adjustment is needed. If the *Width_fact* > 1, it denotes the P/G network does not satisfy the IR drop constraint. So the widths of power wires are broadened according to *Width_fact*. When *Width_fact* is smaller than 1, the width of P/G wire can provide enough voltages. So we can narrow the width to minimize the P/G network wiring resource. The wire sizing method minimizes the used power routing resource with considering IR voltage drop and EM according to a given floorplan. If the constraints are still not satisfied by enlarging the width of the power wire, we will choose a larger power mesh network to evaluate and adjust the width until all constraints are met.

VI. Experimental Results

The proposed method was implemented in C++ language on an Intel Core(TM) 2 Duo Processor 2.5GHz computer with 2G RAM. It was built on the public B*-tree distribution available at [9]. Our experiments were tested on five MCNC benchmark circuits. The resistivity of the two metal layers is 0.075 Ω per square. The IR-drop constraints are $V_{min} = 2.25v$ for power pins and $V_{max} = 0.25v$ for ground pins, and the maximum allowable IR drop is 250mv. We gave each circuit two power pads and randomly assigned the peak current on each P/G pin of the modules which are similar to [1]. In our experimental results, “WL” denotes the wire length, “A” stands for the packing area, “T” gives the run time and “A_p” represents the area of P/G network resources. All the IR drop and EM constraints are satisfied in the following results of P/G aware floorplanners.

A. Effect of pattern-selection and incremental move based P/G network model

Our algorithm uses the pattern selection method which can speed up the optimization process by avoiding repeatedly calculating complex matrix inverse. We compared different floorplanners: (1) PSA floorplanner: plain public SA with B*-tree[9]. (2) SR-FPG in [1]: co-design floorplanner with the power-feasibility consideration using solution space reduction method in [1]; (3) PS_FPG: co-design floorplanner using our pattern-selection based algorithm without considering the wiring resources optimization; (4)PS_FPG^I: co-design floorplanner using our pattern-selection and incremental move based algorithm without considering the wiring resources optimization. Table I shows the comparison results between these approaches. Since the results of SR-FPG are from paper [1] which were run on the different machine, it is not fair to compare the runtime directly. But from the results we can see that the runtime of our co-design using the pattern-selection based algorithm is 4 times of the plain SA based on B*-tree. While it was reported in [1] that the overhead of P/G co-design with floorplan is about 10 times than plain SA based on B*-tree.

Therefore, from this point of view, we can see that our approach can achieve about 2.5 times speed-up to the approach in [1]. For some specific cases, we can see the runtimes of apte and xerox for PS-FPG are improved about 90% than [1]

Our algorithm also adopts a novel design methodology to find an optimized floorplan with a guided incremental floorplan algorithm. Comparing between PS_FPG floorplanner and PS_FPG^I floorplanner which adopts incremental P/G guided moves during the floorplanning, we can see the run time can be furtherly saved about 20% since the P/G guided moves intelligently fix the violated solution so that the useless random search on infeasible solutions are avoided. Unlike [1] which may lose the ability to find the optimal packing due to the reduction of solution space, our incremental approach can maintain the packing quality in a complete solution space.

B. Effect of P/G pin assignment and wire sizing

In our experiments, we also compared another two different floorplanners: (5)PS_FPG^{ICW}: co-design floorplanner using our pattern-selection and incremental move based algorithm with considering the wiring resources optimization in the cost function; (6)PS_FPG^{IW}: our co-design floorplanner using pattern-selection and incremental move based algorithm with the wire sizing and P/G pin assignment method during the floorplanning. From table II, it shows that the wiring resource is optimized 36% by using the cost function method compared with the PS_FPG^I floorplanner. But our approach using the P/G pin assignment and wire sizing methods during the floorplanning can decrease 43% of the P/G network wiring resource compared with the results without considering the wiring resource optimization. And the runtime overhead is acceptable which is about 10% slower than the cost function based approach. Therefore, our co-design floorplanner using the wire sizing and P/G pin assignment method is better than the traditional co-design floorplanner using cost punishment to optimize the wiring resources.

VII. Conclusion

In this paper, we set up a pattern selection scheme for fast signal-integrity estimation. Using pattern selection method can significantly speed up the optimization process. We also propose a guided incremental floorplanning approach to amend

the violations intelligently during the floorplanning process. At the same time, to minimize the area of P/G network, the P/G pin assignment and wire sizing method are also embedded in the floorplanning optimization process. Experimental results show that our design not only significantly speeds up the optimization process, but also optimize the power routing resource with maintaining the quality of the floorplan.

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TABLE I: Comparison between the plain SA with B*-tree representation [9], PS_FPG, the PS_FPG^I and the SR-FPG in [1] (note that the [1] was implemented on a Sun Blade 2000 workstation with one 1GHZ CPU and 8 GB RAM)

circuit	Plain SA with B*-tree			SR_FPG floorplanner[1]			PS-FPG floorplanner			PS_FPG ^I floorplanner		
	WL (mm)	A (mm ²)	T (s)	WL (mm)	A (mm ²)	T (s)	WL (mm)	A (mm ²)	T (s)	WL (mm)	A (mm ²)	T (s)
apte	456.1	49.44	0.83	452	48.8	43.2	479.4	48.12	5.02	470	48.72	4.12
xerox	458.9	22.72	1.51	410	22.4	47.3	431.3	21.18	3.97	412	20.74	3.25
hp	181.2	10.24	0.96	189	11.7	24.0	201.8	10.57	10.6	179.9	10.88	8.31
ami33	59.24	1.28	17.7	73.2	1.2	20.2	64.9	1.23	48.9	61.4	1.22	38.2
ami49	848.5	40.07	95.96	779.9	44.2	450	782.4	48.3	354.6	790.8	48.8	298.7
Comp.	0.98	0.97	0.25	1	1	----	1.01	0.98	1	0.96	0.99	0.80

TABLE II: Comparison between PS_FPG^I, PS_FPG^{ICW} and PS_FPG^{IW}

circuit	PS_FPG ^I floorplanner				PS_FPG ^{ICW} floorplanner				PS_FPG ^{IW} floorplanner			
	WL (mm)	A (mm ²)	A _p (mm ²)	T (s)	WL (mm)	A (mm ²)	A _p (mm ²)	T (s)	WL (mm)	A (mm ²)	A _p (mm ²)	T (s)
apte	470	48.72	1.25	4.12	462	52.45	0.82	12.25	484	50.43	0.742	15.9
xerox	412	20.74	1.16	3.25	412	23.80	0.57	17.31	442	21.74	0.473	20.6
hp	179.9	10.88	0.76	8.13	156.9	10.88	0.37	12.72	157.3	10.63	0.343	21.39
ami33	61.4	1.22	0.141	38.2	62.4	1.42	0.13	49.5	62.67	1.42	0.118	38.6
ami49	790.8	48.8	0.81	298.7	890	41.2	0.72	451.2	884.4	42.72	0.673	349.7
Comp.	1	1	1	1	1.02	1.05	0.64	2.62	1.05	1.02	0.57	2.9